

EXC-8000PCle

**Test and Simulation Carrier Board
for PCIe Systems**

User's Manual



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1 Introduction

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Note: The *EXC-8000PCIe* will not work without the power cable connected. See 1.2 Installation on page 1-6.

1.1 Overview

The *EXC-8000PCIE* carrier board is a multiprotocol PCIe interface board for avionics test and simulation applications. The board holds up to eight independent modules, where each module can be any one of the following types:

M8K429RT5	ARINC 429 multi-channel interface module. This module supports five ARINC 429 channels each of which can be configured in real time as a receive or transmit channel.
M8K708	ARINC 708 interface module. This module supports up to two ARINC 708/453 channels for the Weather Radar Display Databus. Each channel is selectable as transmit or receive and implements a 64K-word FIFO and supports polling and/or interrupt driven operation.
M8KH009	H009 interface module. This module supports a fully functional H009 channel (CCC, multi-PU,MON) and a concurrent Bus Monitor. This is a double-sized module and occupies two modules locations.
M8K717-Nx	ARINC 717 interface module. This module supports two ARINC 717 channels; one receive channel and one transmit channel.
M8K825CAN-S5	ARINC 825 interface module. This module supports up to five ARINC 825 channels.
M8KDiscrete	Discrete I/O interface module. This module supports 10 bi-directional Discretes with TTL (0 to 5 volts) or avionics (0 to 32 volts) voltage levels.
M8K1553Px	MIL-STD-1553 interface module. This module operates as a Bus Controller, up to 32 Remote Terminals and as a Bus Monitor. It supports an Internal Concurrent Monitor in RT and BC/RT modes.
M8K1553PxS	Same as the M8K1553Px, but for only one Remote Terminal at a time (single function) and one mode at a time (no BC/RT mode) and no error injection.
M8K1553PxM	Monitor-only version of the M8K1553Px.
M8K1553PxSM	Monitor-only version of the M8K1553PxS.
M8K1553MCH	MIL-STD-1553 MCH interface module. This module operates as a Bus Controller, Remote Terminal and as a Bus Monitor. This is a double-sized module and occupies two modules locations.
M8K1760Px	MIL-STD-1760 interface module. This module operates as a Bus Controller, up to 32 Remote Terminals and as a Bus Monitor. It supports an Internal Concurrent Monitor in RT and BC/RT modes.
M8K1760PxS	Same as the M8K1760Px, but for only one Remote Terminal at a time (single function) and one mode at a time (no BC/RT mode) and no error injection.
M8K1760PxM	Monitor-only version of the M8K1760Px.
M8K1760PxSM	Monitor-only version of the M8K1760PxS.
M8KMMSI-R5	Mini Munitions Store Interface module. This module supports RT, BC/ Concurrent-RT/ Concurrent Monitor and Bus Monitor modes. Up to 5 hub ports EBR-1553 (10 Mbps MIL-STD-1553 protocol using RS-485 transceivers) and a composite monitor output (cBM).
M8KSerial-Jx	Serial communications interface module. This module supports two independent channels of serial communications, each of which can be selected as RS485, RS422 or RS232.

M8KADDA	Multichannel digital-to-analog and analog-to-digital interface module. This module supports up to 10 single ended, or 5 differential, digital-to-analog (DAC) output channels, as well as 5 single ended or 5 differential analog-to-digital (ADC) input channels.
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Excaltibur will be adding modules to those listed above, increasing the board's flexibility even further.

You can choose to populate the board with different types of modules or with multiple modules of the same type. For example, populating the board with eight *M8K429RT5* modules will give you *forty* programmable channels. All modules come with Windows drivers, including source code.

1.1.1 Board Features

General Features

- Supported protocols (on up to 8 removable modules):
 - ARINC 429/575 (5 channels per module)
 - ARINC 708/453 (2 channels per module)
 - ARINC 717 (2 channels per module)
 - ARINC 825 (CAN) (5 channels per module)
 - MIL-STD-1553 (single or multifunction)
 - MIL-STD-1760 (single or multifunction)
 - H009 (double-sized module with one channel)
 - Discrete I/O (10 channels per module)
 - Serial RS-485/RS-422/RS-232 (2 channels per module)
 - MMSI/AS5652 (5 channels per module)
 - A/D and D/A (5 differential or 10 single ended channels)
- 16-bit Count Down Timer
 - 1–65,635 μ s resolution
 - Interrupt or global reset upon count down

IRIG B Time Code Input

- Carrier wave:
 - 1KHz Amplitude modulated sine wave
- Rate Designation: 100 peaks per second
- Modulation ratio: 3:1
- Input Amplitude: 0.8–3.5 V_{pp} (3 V_{pp} Typ)
- Coded Expressions supported:
 - BCD time-of-year code word
 - Control functions
 - Straight Binary Seconds (SBS) time-of-day
- Application:
 - Synchronization of Time Tags, display and IRIG B time

Physical Characteristics

- Dimensions: 188.0 mm x 98.5 mm
- Weight: 135 g (without modules)

Operating Environment

- Temperature: 0°–70°C standard temperature
-40° to +85°C extended temperature (optional)
- Humidity: 5%–90% noncondensing
- MTBF: 188,540 hours at 25°C, G_F, S217F

Host Interface

- PCI Express compliance: x1 lane PCIe v1.1
- Memory space occupied: 64 MB
- Interrupts: INTA# virtual wire
- Power: Depends on configuration. For more details, see **3.5 Power Requirements** on page 3-17.

Software Support

- *Excalibur Carrier Board Software Tools*:
 - Intuitive and flexible API with source code
 - Compatible with 32/64-bit Windows 7/8/10 & Linux kernel 3.x/4.x
 - Includes application interface for NI LabView & CVI
- *Exalt Plus*: Excalibur Analysis Laboratory Tools for Windows (optional)

System Requirements

- Operating system: 64-bit Windows
- CPU: Intel® Core™ i3 Processors or equivalent (recommended)
- RAM: 8 GB (recommended)

1.1.2 Block Diagram

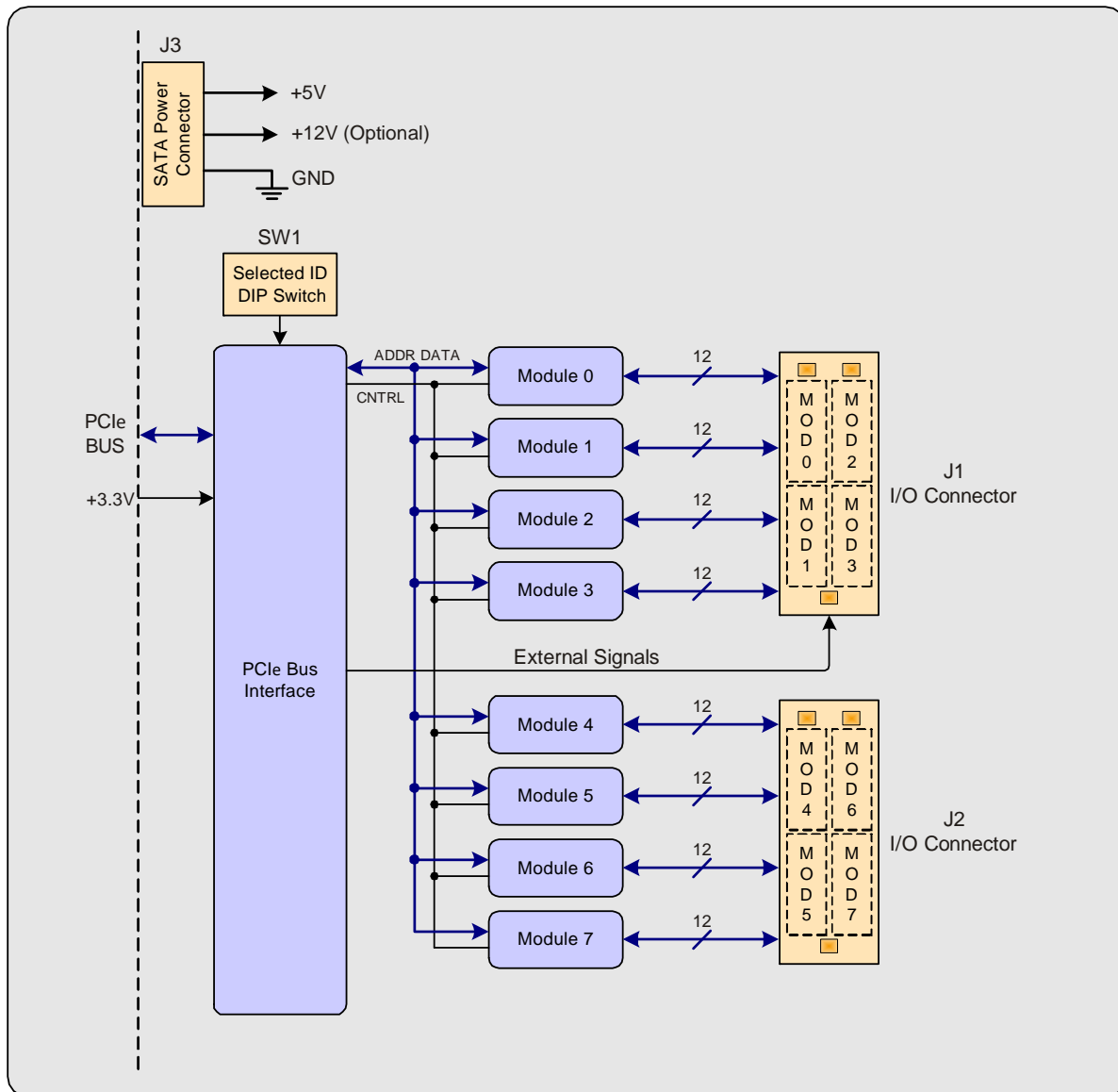


Figure 1-1 Block Diagram

1.2 Installation

For hardware and software installation instructions, see **Installation Instructions.pdf** in the root folder of the installation CD. When downloading new software from the Excalibur website, **Installation Instructions.pdf** is contained in the zip file.

The *Excalibur Installation CD* you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. For more details, see **Installation Instructions.pdf**. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.3 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, visit the [Technical Support](#) page of our website (www.mil-1553.com). You can also contact us by phone. To find the location nearest you, visit to the [Contact Us](#) page of our website. Before contacting Technical Support, please see [Information Required for Technical Support](#).

2 PCI Architecture

Chapter 2 describes the PCI Express architecture. The following topics are covered:

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2.1 Memory Structure

The *EXC-8000PCIe* requests the following memory blocks:

- The first memory block (Base Address Register 0) is 64 MB and contains the memory space for the modules on the board. For more information, see **2.8 Module Memory Space Map** on page 2-19.
- The second memory block (Base Address Register 1) is 32 KB in size and contains the DMA registers. DMA functionality is described in the software tools programmer's reference of each of your board's modules.
- The third memory block (Base Address Register 2) is 8 KB in size and contains the Global registers. For more information, see **2.5 Board Global Registers Map** on page 2-9.

2.2 PCI Configuration Space Header

The board includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

The following figure shows the PCI Express Configuration Space Header for PCI Express:

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H			
Reserved = 0s				38 H			
Reserved = 0s			Cap. pointer	34 H			
Expansion ROM Base Address (Not Used)				30 H			
Subsystem ID		Subsystem Vendor ID		2C H			
Cardbus CIS Pointer – Not Used = 0s				28 H			
Base Address Register #5 – Not Used				24 H			
Base Address Register #4 – Not Used				20 H			
Base Address Register #3 – Reserved				1C H			
Base Address Register #2 – Global Registers				18 H			
Base Address Register #1 – DMA Registers				14 H			
Base Address Register #0 – Module Memory Space				10 H			
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H			
Class Code			Rev ID	08 H			
Status Register		Command Register		04 H			
Device ID		Vendor ID		00 H			
31	24	23	16	15	08	07	00

Figure 2-1 PCI Configuration Space Header

2.3 PCI Configuration Registers

2.3.1 Vendor Identification Register (VID) Address: 00–01 (H)

Power-up value 1405 H
Size: 16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems.

2.3.2 Device Identification Register (DID) Address: 02–03 (H)

Power-up value: E800 H
Size: 16 bits

The Device Identification register contains the board's device identification number.

2.3.3 PCI Command Register (PCICMD) Address: 04–05 (H)

Power-up value: 0000 H
Size: 16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	Reserved	Set to 0s
09	Fast Back-to Back Enable	Always set to 0
08	System Error Enable	Always set to 0
07	Address Stepping Support	Always set to 0
06	Parity Error Enable	Always set to 0
05	VGA Palette Snoop Enable	Always set to 0
04	Memory Write and Invalidate Enable	Always set to 0
03	Special Cycle Enable	Always set to 0
02	Bus Master Enable	Always set to 1
01	Memory Access Enable	Always set to 1
00	I/O Access Enable	Since the board does not use I/O space, the value of this register is ignored.

Table 2-1 PCI Command Register

2.3.4 PCI Status Register (PCISTS) Address: 06–07 (H)

Power-up value: 0080 H

Size: 16 bits

The PCI Status register contains the PCI status information for PCI Express.

Bit	Bit Name	Description
15	Detected Parity Error	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	Signaled System Error	Not used
13	Received Master Abort	This bit is set when the device receives a master abort to terminate a transaction. This bit can be reset by writing a 1 to this location.
12	Received Target Abort	Not used
11	Signaled Target Abort	Not used
09-10	Device Select (DEVSEL#) Timing Status	Set to 00 (fast timing)
08	Data Parity Reported	Not used
07	Fast Back-to-Back Capable	Set to 0
06	UDF Supported	Set to 0
05	66MHz capable	Set to 0
04	Capability List enable	Set to 1
03	Interrupt Status	This bit is set when an interrupt is received.
00-02	Reserved	

Table 2-2 PCI Status Register

2.3.5 Revision Identification Register (RID) Address: 08 (H)

Power-up value: 01 H

Size: 8 bits

The Revision Identification register contains the revision identification number of the board.

2.3.6 Class Code Register (CLCD) Address: 09–0B (H)**Power-up value:** FF0000 H**Size:** 24 bits

The Class code Register value indicates that the board does not fit into any of the defined class codes.

2.3.7 Cache Line Register Size Register (CALN) Address: 0C (H)**Power-up value:** 10 H**Size:** 8 bits

Not used

2.3.8 Latency Timer Register (LAT) Address: 0D (H)**Power-up value:** 00 H**Size:** 8 bits

Not used

2.3.9 Header Type Register (HDR) Address: 0E (H)**Power-up value:** 00 H**Size:** 8 bits

The board is a single function PCI device.

2.3.10 Built-In Self-Test Register (BIST) Address: 0F (H)**Power-up value:** 00 H**Size:** 8 bits

The Built-In Self-Test register is not implemented in the board.

2.3.11 Base Address Registers (BADR) Address: 10, 14, 18, 1C, 20, 24 (H)**Power-up value:** 00000000 H for each**Size:** 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

Three memory pages are required by the board: one for the module memory space, one for the Global Registers and one for the DMA registers.

Register	Offset	Size	Function
Base Address 0	10 H	64 MB	Module memory space
Base Address 1	14 H	32 KB	DMA registers
Base Address 2	18 H	8 KB	Global registers

Table 2-3 Base Address Registers Definition

Note: Each Base Address Register contains 32 bits. Since the PCI Express board uses 64-bit address space, each memory page covers two base addresses (0 – 1, 2 – 3, 4 – 5).

The following table describes the bits of the Base Address Register.

Bit	Description
04-31	Address of memory region (with lower 4 bits removed)
03	Always 1 – memory is prefetchable
01-02	Always 2 – memory may be mapped anywhere within the 64 bit memory space
00	Always 0 – indicates memory space

Table 2-4 Base Address Register

2.3.12	Cardbus CIS Pointer	Address: 28 (H)
	Power-up value:	00000000 H
	Size:	32 bits
The Cardbus Pointer is not implemented on the board.		
2.3.13	Subsystem ID	Address: 2C (H)
	Power-up value:	0000 H
	Size:	16 bits
2.3.14	Subvendor ID	Address: 2E (H)
	Power-up value:	0000 H
	Size:	16 bits
2.3.15	Expansion ROM Base Address Register (XROM)	Address: 30 (H)
	Power-up value:	00000000 H
	Size:	32 bits

The Expansion ROM Space is not implemented on the board.

2.3.16 PCI Capabilities Pointer Address: 34 (H)**Power-up value:** 50 H**Size:** 8 bits

The PCI Capabilities Pointer (Cap. Pointer) indicates the location of the PCI Capabilities Identification (ID) Register. The Capabilities ID Register stores a pointer to a structure within the configuration space. With a known Capabilities ID value, the associated structure can be found during the scanning process.

2.3.17 Interrupt Line Register (INTLN) Address: 3C (H)**Power-up value:** 00 H**Size:** 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For x86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 1 to F (H) correspond with the IRQ numbers 1 through 15, and the values from 10(H) to FE (H) are reserved. The value of 255 signifies either “unknown” or “no connection” for the system interrupt.

2.3.18 Interrupt Pin Register (INTPIN) Address: 3D (H)**Power-up value:** 01 H**Size:** 8 bits

Set to INTA#

2.3.19 Minimum Grant Register (MINGNT) Address: 3E (H)**Power-up value:** 00 H**Size:** 8 bits

The Minimum Grant register is not implemented on the board.

2.3.20 Maximum Latency Register (MAXLAT) Address: 3F (H)**Power-up value:** 00 H**Size:** 8 bits

The Maximum Latency register is not implemented on the board.

2.4 Board Global and DMA Registers Memory Space Map

The DMA Registers are mapped as follows.



Figure 2-2 DMA Registers Memory Space Map

The Global Registers are mapped as follows.

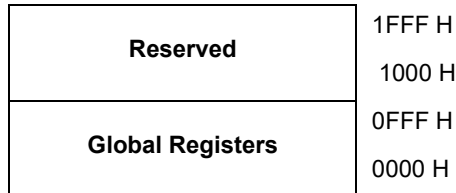


Figure 2-3 Global Registers Memory Space Map

2.5 Board Global Registers Map

The board global registers reside in the second memory block.

Reserved																40-0FFF H	
Module 7 Info																3E H	
Module 6 Info																3C H	
Module 5 Info																3A H	
Module 4 Info																38 H	
Reserved																30-36 H	
General Purpose Timer																28 H	
Reserved											Timer Control					26 H	
Timer Preload																24 H	
Timer Prescale																22 H	
FPGA Revision																20 H	
Control Functions Low																1E H	
Reserved							Control Functions Hi									1C H	
IRIG B Time Minutes			IRIG B Time Seconds													1A H	
IRIG B Time Days								IRIG B Time Hours								18 H	
IRIG B Time SBS Low																16 H	
Reserved							Sync IRIG B			Reserved					SBS Hi ¹	14 H	
Reserved																12 H	
Time Tag Clock Select																10 H	
Module 3 Info																0E H	
Module 2 Info																0C H	
Module 1 Info																0A H	
Module 0 Info																08 H	
Interrupt Reset																06 H	
Interrupt Status																04 H	
Software Reset																02 H	
Board ID																00 H	
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Figure 2-4 Global and IRIG B Registers Map

1. IRIG B Time SBS Hi Register

2.5.1 Board Identification Register

Address: 00 (H)
Length: 16 bits

Read only The Board Identification register comprises the following identification items.

Bit	Description
04-15	Hard coded to the value 8E0 H
00-03	Selected ID See 3.3.1 Select ID DIP Switch [SW1] on page 3-3.

Table 2-5 Board Identification Register

2.5.2 Software Reset Register

Address: 02 (H)
Length: 16 bits

Read/Write The Software Reset register performs reset operations of the modules. Individual modules may be reset.

Bit 04, the Global Time Tag reset bit, resets all the module's Time Tag counters.

Bit	Description
09-15	Reserved – set to 0
08	Module 7 reset 1 = reset module 0 = no effect
07	Module 6 reset 1 = reset module 0 = no effect
06	Module 5 reset 1 = reset module 0 = no effect
05	Module 4 reset 1 = reset module 0 = no effect
04	Global time tag reset 1 = reset all time tag counters 0 = no effect
03	Module 3 reset 1 = reset module 0 = no effect
02	Module 2 reset 1 = reset module 0 = no effect
01	Module 1 reset 1 = reset module 0 = no effect
00	Module 0 reset 1 = reset module 0 = no effect

Table 2-6 Software Reset Register

2.5.3 Interrupt Status Register

Address: 04 (H)
Length: 16 bits

Read only The Interrupt Status register indicates which modules are currently interrupting or if the General Purpose Timer has produced an interrupt.

Bit	Description
09-15	Reserved – set to 0
08	1 = indicates that module 7 is interrupting
07	1 = indicates that module 6 is interrupting
06	1 = indicates that module 5 is interrupting
05	1 = indicates that module 4 is interrupting
04	1 = indicates that an interrupt was generated by the General Purpose Timer [See 2.7 Global Timer Registers on page 2-17]
03	1 = indicates that module 3 is interrupting
02	1 = indicates that module 2 is interrupting
01	1 = indicates that module 1 is interrupting
00	1 = indicates that module 0 is interrupting

Table 2-7 Interrupt Status Register

2.5.4 Interrupt Reset Register

Address: 06 (H)
Length: 16 bits

Write only The Interrupt Reset register resets the interrupting modules by writing to the relevant bits of the register.

Bit	Description
09-15	Reserved – set to 0
08	1 = Resets module 7 interrupt 0 = No effect
07	1 = Resets module 6 interrupt 0 = No effect
06	1 = Resets module 5 interrupt 0 = No effect
05	1 = Resets module 4 interrupt 0 = No effect
04	1 = Resets General Purpose Timer interrupt 0 = No effect
03	1 = Resets module 3 interrupt 0 = No effect
02	1 = Resets module 2 interrupt 0 = No effect
01	1 = Resets module 1 interrupt 0 = No effect
00	1 = Resets module 0 interrupt 0 = No effect

Table 2-8 Interrupt Reset Register

2.5.5 Module Info Registers for Modules 0 – 3 **Address: 08, 0A, 0C, 0E (H)**
Length 16 bits each

Read only The Module Info Registers provide identification information for each of the modules.

Bit	Description
05-15	Module number 00 H = Module 0 Info register 01 H = Module 1 Info register 02 H = Module 2 Info register 03 H = Module 3 Info register
00-04	Module type 23 H = <i>M8K1553MCH</i> module 24 H = <i>M8K429RT5</i> module 25 H = <i>M8K1553Px</i> or <i>M8K1760Px</i> module 26 H = <i>M8KMMSI</i> module 27 H = <i>M8K708</i> module 28 H = <i>M8K825CAN</i> module 29 H = <i>M8KH009</i> module 2A H = <i>M8KADDA</i> module 2D H = <i>M8KDiscrete</i> module 32 H = <i>M8KSerial</i> module 37 H = <i>M8K717</i> module 1F H = no module installed

Table 2-9 Module Info Registers

2.5.6 Module Info Registers for Modules 4 – 7 **Address: 38, 3A, 3C, 3E (H)**
Length 16 bits each

Read only The Module Info Registers provide identification information for each of the modules.

Bit	Description
05-15	Module number 04 H = Module 4 Info register 05 H = Module 5 Info register 06 H = Module 6 Info register 07 H = Module 7 Info register
00-04	Module type 23 H = <i>M8K1553MCH</i> module 24 H = <i>M8K429RT5</i> module 25 H = <i>M8K1553Px</i> or <i>M8K1760Px</i> module 26 H = <i>M8KMMSI</i> module 27 H = <i>M8K708</i> module 28 H = <i>M8K825CAN</i> module 29 H = <i>M8KH009</i> module 2A H = <i>M8KADDA</i> module 2D H = <i>M8KDiscrete</i> module 32 H = <i>M8KSerial</i> module 37 H = <i>M8K717</i> module 1F H = no module installed

Table 2-10 Module Info Registers

2.5.7 Time Tag Clock Select Register**Address: 10 (H)**
Length 16 bits

Read/Write The Time Tag Clock Select Register is used to set either an internal (1 MHz) or external source for the board's Global Time Tag Clock. External Signals are transmitted via connector J1. See **3.4.2 Communications I/O Connectors [J1 and J2]** on page 3-6.

Bit	Description
01-15	Reserved – set to 0
00	Time Tag Clock Select 1 = External Source 0 = Internal Source [Default]

Table 2-11 Time Tag Clock Select Register**2.5.8 FPGA Revision Register****Address: 20 (H)**
Length 16 bits

Read only The FPGA Revision register contains the FPGA revision of the board.

2.6 IRIG B Global Registers

The *EXC-8000PCIe* is able to receive and decode standard serial IRIG B time code format signals via connector J1. The signals are 1 KHz carrier wave, sine wave, amplitude modulated, 100 peaks per second. See External Signals in **3.4.2 Communications I/O Connectors [J1 and J2]** on page 3-6.

The IRIG B signal, which contains 3 types of words within each Time Code Frame, can be used to synchronize the Time Tags of the modules on the board.

- 1st Word Time-of-year in binary coded decimal (BCD) notation in hours, minutes and seconds.
- 2nd Word Set of bits reserved for decoding various control, identification and other special purpose functions.
- 3rd Word Seconds-of-day weighted in straight binary seconds (SBS) notation

These three words can be stored and displayed in the IRIG B global registers 14 - 1E (H).

See **Figure 2-4 Global and IRIG B Registers Map** on page 2-9 for the location of the registers on the memory map.

Note: The synchronization of IRIG B time can take up to two seconds. IRIG B functions are meant to be used on an occasional basis, not on a constant basis.

2.6.1 Sync IRIG B Register

Address: 14 (H)
Bits: 08 – 10

Read/Write The 3-bit Sync IRIG B register controls the synchronization of a module's Time Tags relative to the IRIG B input signal and the display of the IRIG B time within the IRIG B time registers.

Bit	Description
10	1 Set by board to indicate that the current IRIG B time has been stored in the IRIG B registers
	0 No IRIG B time has been stored in the IRIG B registers. This bit must be reset by the user after the board has written a '1'.
09	1 Stores and displays the IRIG B time and control functions into the 6 IRIG B registers (14-1E [H]) corresponding to the previous valid IRIG B message. If bit 08 is set, then the IRIG B time will be stored at the same time that the Time tags are reset. To calculate the realtime to which the Time tags are synchronized the user will need to add '1' to the value of the IRIG B time stored into these registers.
	0 The previous valid IRIG B message should not be stored in the IRIG B registers. This bit will be automatically reset by the board after the storage of the IRIG B time.
08	1 Resets and synchronizes Time Tags of all the modules to the next rising edge of the on-time Reference Point Pr of the IRIG B signal. Also sets Bit 09 to a value of '1' in order to store and display the IRIG B time and control functions into the 6 IRIG B registers.
	0 No reset/synchronization of Time tags relative to the Pr of the IRIG B signal. This bit will be automatically reset by board after reset of time tags

Table 2-12 Sync IRIGB Register

Note: All bits are read and write.

2.6.2 IRIG B Time SBS High Register

Address: 14 (H)
Bit: 0

Read only The IRIG B Time SBS High register contains the MSB of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.6.3 IRIG B Time SBS Low Register

Address: 16 (H)
Bits: 15 – 0

Read only The IRIG B Time SBS Low register contains the lower 16 bits of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.6.4 IRIG B Time Days Register

Address: 18 (H)
Bits: 15 – 6

Read only The IRIG B Time Days register contains the days value of the BCD time-of-year subword within the IRIG B coded message.

- 2.6.5 IRIG B Time Hours Register** **Address: 18 (H)**
Bits 5 – 0
- Read only** The IRIG B Time Hours register contains the hours value of the BCD time-of-year subword within the IRIG B coded message.
- 2.6.6 IRIG B Time Minutes Register** **Address: 1A (H)**
Bits 14 – 8
- Read only** The IRIG B Time Minutes register contains the minutes value of the BCD time-of-year subword within the IRIG B coded message.
- 2.6.7 IRIG B Time Seconds Register** **Address: 1A (H)**
Bits 6 – 0
- Read only** The IRIG B Time Seconds register contains the seconds value of the BCD time-of-year subword within the IRIG B coded message.
- 2.6.8 Control Functions Registers** **Hi Register Address: 1C (H) / Bits 10 – 0**
Low Register Address: 1E (H) / Bits 15 – 0
- Read only** The IRIG B time code formats reserve 27 bits known as Control Functions. The Control Functions are for user-defined encoding of various control, identification or other special purpose functions. No standard coding system exists. The control bits may be programmed in any predetermined coding system.
- 2.6.9 FPGA Revision Register** **Address: 20 (H)**
Bits 15 – 0
- Read only** The FPGA Revision register contains the FPGA revision of the board.

2.7 Global Timer Registers

See **Figure 2-4 Global and IRIG B Registers Map** on page 2-9 for location of the registers on the memory map.

2.7.1 Timer Prescale Register

Address: 22 (H)
Bits: 15 – 0

Read/Write The Timer Prescale Register defines the resolution of the General Purpose Timer. It is based on the Global Time Tag Clock (nominally 1 MHz) and thus will give the General Purpose Timer resolution as follows:

Timer Prescale Register Value (DEC)	General Purpose Time Resolution (μ sec)
0 or 1	1 (default)
2	2
3	3
•	•
•	•
•	•
10	10
•	•
•	•
•	•
65535	65535

Table 2-13 Timer Prescale/General Purpose Timer Resolution

Note: The Timer Prescale register can only be changed when the timer has been stopped.

2.7.2 Timer Preload Register

Address: 24 (H)
Bits: 15 – 0

Read/Write The value stored in the Timer Preload Register sets the starting count value for the General Purpose Timer from which it will start to count down. The Timer Preload Register can only be changed while the timer is stopped and has a maximum count value of 65535.

Note: The General Purpose Timer will not start counting if a value of zero is stored into the Timer Preload Register.

Default value: 00 00

2.7.3 Timer Control Register

Address: 26 (H)
Bits: 3 – 0

Read/Write The Timer Control Register is used to control the General Purpose Timer register. The value stored in bits 01 to 03 take effect when the General Purpose timer reaches a value of zero. Bit 00 is used to start and stop the General Purpose

Timer. The values of bits 01 – 03 can only be changed when the General Purpose Timer register is stopped.

Default value: 00 00

Bit	Description		
04-15	Reserved - set to 0		
03	Global reset on count completed	1 0	Causes global reset of all installed modules No effect
02	Interrupt on count completed	1 0	Output an interrupt (see 2.5.3 Interrupt Status Register on page 2-11) No effect
01	Reload mode	1 0	Reload mode Non-reload/One-shot mode
00	Start/Stop	1 0	Start Stop

Table 2-14 Timer Control Register

2.7.4 General Purpose Timer Register

Address: 28 (H)
Bits 15 – 0

Read Only The General Purpose Timer Register stores the current count value of the General Purpose Timer. The General Purpose Timer is controlled by the Timer Control Register. When the General Purpose Timer is started it will count down to zero, at which point either an interrupt can be generated and or all installed modules can be reset.

If the General Purpose Timer is in reload mode then the current value in Timer Preload Register will be stored into the General Purpose Timer and the timer will start to count down from this value.

If the General Purpose Timer is in non-reload / one shot mode, when it reaches zero it will stop and a value of zero will be displayed in the General Purpose Timer Register. In this case bit 00 (Start/Stop bit) of the Timer Control Register will automatically be set to zero in this case. If the General purpose Timer Register is then started it will start to count from the current Timer Preload Register value automatically (without the need to do a write to the Timer Preload Register).

At any point in time, the General Purpose Timer can be stopped at the current count value. When a start is then issued, the General purpose Timer will start to count down from this current count value. If the user wishes to stop the counter and start from the original preload value or from a new preload value, this value will need to be rewritten into the Timer Preload register prior to the restarting of the General Purpose Timer register.

Note: The maximum clock period of the General Purpose Timer is 4295 seconds (1 hour, 11min & 35 Seconds).

2.8 Module Memory Space Map

The module memory space map resides in the first memory block. Each module is allocated a space of 128 KB which is mapped as shown in **Figure 2-5 Module Memory Space Map**. (See **Chapter 4 Ordering Information** for information on the available modules for this carrier board.)

Reserved	3FFF FFFF H 0010 0000 H
Module #7	FFFFF H E0000 H
Module #6	DFFFF H C0000 H
Module #5	BFFFF H A0000 H
Module #4	9FFFF H 80000 H
Module #3	7FFFF H 60000 H
Module #2	5FFFF H 40000 H
Module #1	3FFFF H 20000 H
Module #0	1FFFF H 00000 H

Figure 2-5 Module Memory Space Map

3 Mechanical and Electrical Specifications

Chapter 3 describes the mechanical and electrical specifications of the *EXC-8000PCIe* carrier board. The following topics are covered:

3.1 Board Layout	3-2
3.2 LED Indicators	3-3
3.3 DIP Switches	3-3
3.3.1 Select ID DIP Switch [SW1]	3-3
3.4 Connectors	3-5
3.4.1 SATA Connector [J3]	3-5
3.4.2 Communications I/O Connectors [J1 and J2]	3-6
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3.4.2.2 Adapter Cable	3-13
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3.4.3.1 Synchronizing with an External Source	3-16
3.4.3.2 Synchronizing Between Boards	3-17
3.5 Power Requirements	3-17

3.1 Board Layout

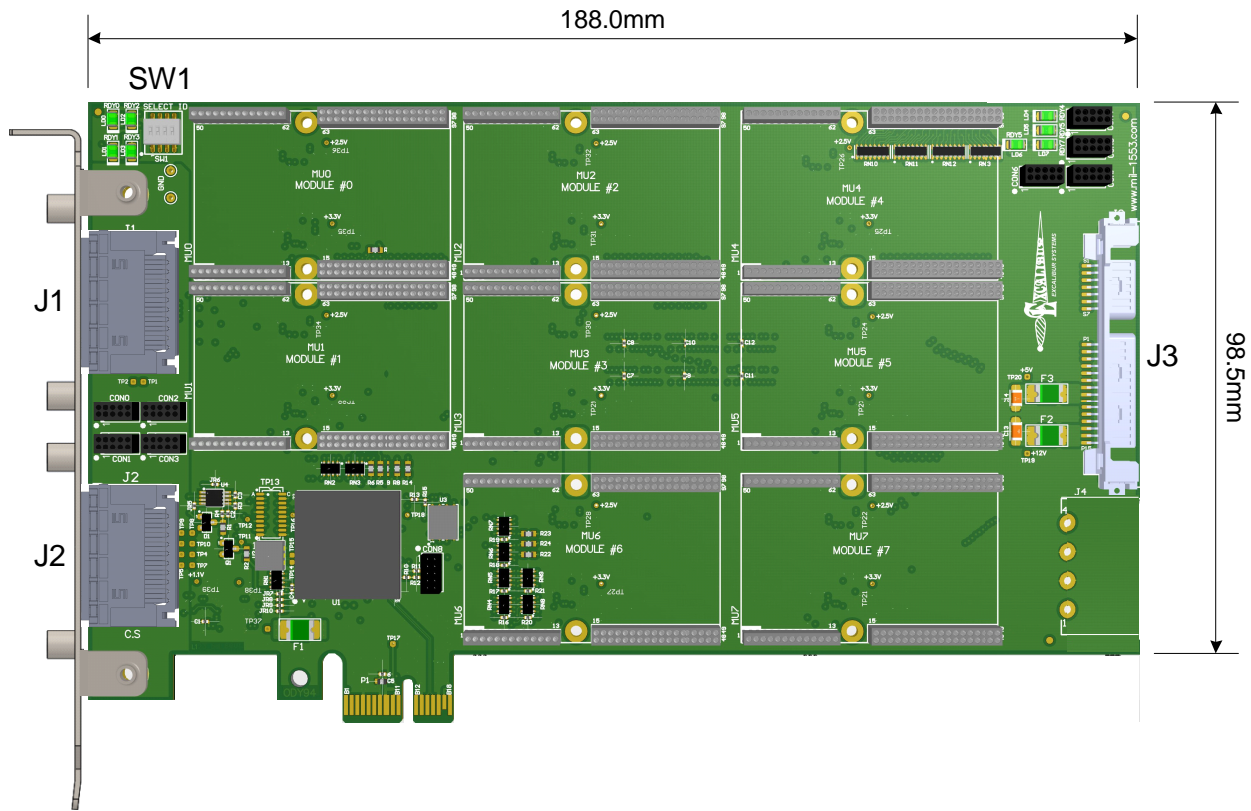


Figure 3-1 Board Layout

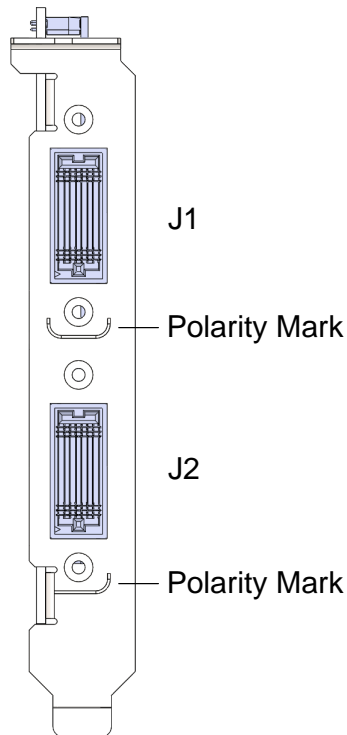


Figure 3-2 Board PC Bracket – Front View

3.2 LED Indicators

The board contain eight LEDs.

LED	Name	Indication
LD0	RDY0	Module 0 Ready
LD1	RDY1	Module 1 Ready
LD2	RDY2	Module 2 Ready
LD3	RDY3	Module 3 Ready
LD4	RDY4	Module 4 Ready
LD5	RDY5	Module 5 Ready
LD6	RDY6	Module 6 Ready
LD7	RDY7	Module 7 Ready

Table 3-1 Led Indicators

3.3 DIP Switches

The board contains one DIP switch (SW1).

3.3.1 Select ID DIP Switch [SW1]

This four contact DIP switch provides the board's 'Selected ID.' It represents a four bit number of which position #1 is the most significant bit. When a specific bit of the switch is:

- **Off** – a value of “1” will be set for that bit
- **On** – a value of “0” will be set for that bit

Multiple Board Applications

To provide a unique Selected ID, to identify a board by the application software in a multiple board application, the DIP switch should be set differently for each board in the same computer. For example:

	For Board ID#1	For Board ID#3
Bit 1	On	On
Bit 2	On	On
Bit 3	On	Off
Bit 4	Off	Off

Table 3-2 DIP Switch Settings for Unique Selected ID

For multiple board applications, each board's device number may be set by using the Excalibur configuration utility program provided with the drivers, and by setting the Unique ID to match that set on the DIP switch shown in Figure 3-3.

Select ID	Bit 1	Bit 2	Bit 3	Bit 4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1

Table 3-3 Selected ID Bits

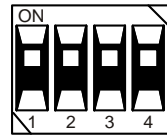


Figure 3-3 DIP Switch SW1 with All Switches Set to ON (Selected ID#0)

3.4 Connectors

3.4.1 SATA Connector [J3]

The power section of this connector mates with the standard PC SATA power supply cable. The signal pins are not connected on the board.

Note: The *EXC-8000PCIe* board will not work without the power cable connected.

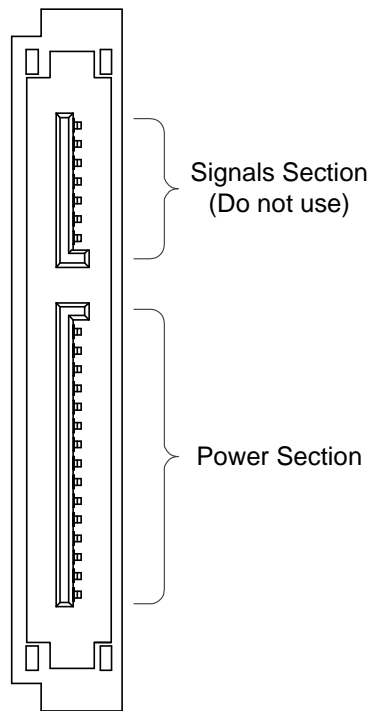


Figure 3-4 15+7-Pin Male SATA Connector [J3] – Front View

Pin	Signal
S1	N/C ¹
S2	N/C
S3	N/C
S4	N/C
S5	N/C
S6	N/C
S7	N/C
P1	N/C
P2	N/C
P3	N/C
P4	GND
P5	GND
P6	GND
P7	+5V
P8	+5V
P9	+5V
P10	N/C
P11	N/C
P12	N/C
P13	+12V
P14	+12V
P15	+12V

Table 3-4 15+7-Pin Male SATA Connector Pinouts

(Optional, for future use)

1. N/C = Not connected.

3.4.2 Communications I/O Connectors [J1 and J2]

The *EXC-8000PCIE* has two 160-pin HD, female I/O connectors mounted on the front panel, P/N: Samtec SEAF8-20-1-S-08-2-RA. Adapter cables can be ordered from Excalibur that terminate in separate connectors for each module installed on the board. See **3.4.2.2 Adapter Cable** on page 3-13.

For those who would like to build their own adapter cable, the mating connector assembly, P/N: Excalibur EXC-8000CON, can be ordered separately. The EXC-8000CON assembly includes the mating connector (P/N: Samtec SEAM8-20-S05.0-S-08-2-K) soldered on to a flexible PCB. See **3.4.2.3 Adapter Cable EXC-8000CON Assembly** on page 3-14.

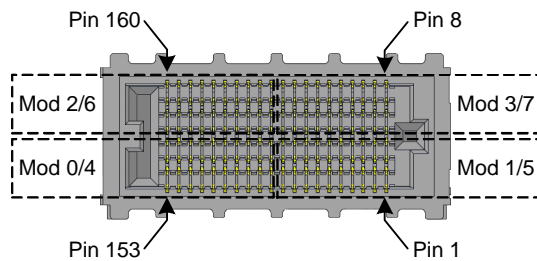


Figure 3-5 J1/J2 Connector – Front View

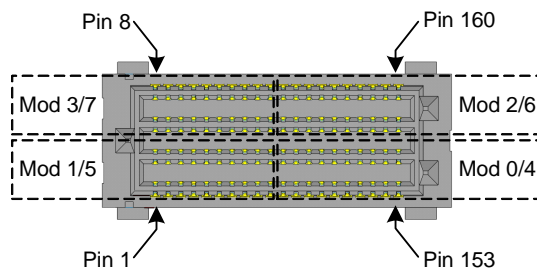


Figure 3-6 J1/J2 Mating Connector – Front View

The pinouts of the J1 and J2 connectors vary depending on the modules installed on the board. Each of the four sections of the J1 and J2 connectors passes the signals of one of the board's removable modules. Connector J1 passes the signals for modules 0–3, and Connector J2 passes the signals for modules 4–7. Connector J1 also passes the External Signals. See Figure 1-1 and Figure 3-1.

Tables 3-5 through 3-10 list the pinouts for the J1 and J2 connectors and the pinouts of the terminating connectors of Excalibur's adapter cable.

These tables have two purposes: (1) To identify the signal on each pin of the J1 and J2 connectors and (2) to build an adapter cable using the Excalibur's mating connector assembly (P/N: EXC-8000CON). The letter-number combinations in the left side of these tables specify the soldering hole numbers in the mating connector assembly. These letter-number combinations are for building an adapter cable. The numbers in parentheses specify the pin numbers of the J1 and J2 connectors.

For more information on the adapter cable, see **3.4.2.2 Adapter Cable** on page 3-13.

Table 3-5 lists the pinouts for the *M8K429RT5*, *M8K717*, *M8K825CAN*, *M8KDiscrete*, *M8KSerial* and *M8KMMSI* modules.

P1/P2 Mating Connector Through-hole Soldering Pad# and J1/J2 On-board Connector Pin# (in Parenthesis)				Module Signal Names									
Modules 0 and 4	Modules 1 and 5	Modules 2 and 6	Modules 3 and 7	HDB 15-pin Adapter Cable Pin#	M8K429RT5	M8K717	M8K825CAN	M8KDiscrete	M8KSerial RS-232	M8KSerial RS-422	M8KSerial RS-485	M8KMMSI	
A1L (100)	B1L (4)	C1L (102)	D1L (6)	2	CH0L	N/C	CH0L	DIO_0	N/C	Ch0_422T_H	Ch0_485_H	CH0L	
A1H (108)	B1H (12)	C1H (110)	D1H (14)	3	CH0H	N/C	CH0H	DIO_1	Ch0_232T	Ch0_422T_L	Ch0_485_L	CH0H	
A2L (98)	B2L (2)	C2L (117)	D2L (21)	4	CH1L	N/C	CH1L	DIO_2	Ch0_232R	Ch0_422R_H	N/C	CH1L	
A2H (106)	B2H (10)	C2H (125)	D2H (29)	5	CH1H	N/C	CH1H	DIO_3	N/C	Ch0_422R_L	N/C	CH1H	
A3L (115)	B3L (19)	C3L (119)	D3L (23)	7	CH2L	N/C	CH2L	DIO_4	GND	GND	GND	CH2L	
A3H (123)	B3H (27)	C3H (127)	D3H (31)	8	CH2H	N/C	CH2H	DGND_04	SHIELD	SHIELD	SHIELD	CH2H	
A4L (138)	B4L (42)	C4L (142)	D4L (46)	9	CH3L	N/C	CH3L	DIO_5	N/C	Ch1_422T_H	Ch1_485_H	CH3L	
A4H (130)	B4H (34)	C4H (134)	D4H (38)	10	CH3H	N/C	CH3H	DIO_6	Ch1_232T	Ch1_422T_L	Ch1_485_L	CH3H	
A5L (155)	B5L (59)	C5L (159)	D5L (63)	11	CH4L	Ch717TxL	CH4L	DIO_7	Ch1_232R	Ch1_422R_H	N/C	CH4L	
A5H (147)	B5H (51)	C5H (151)	D5H (55)	12	CH4H	Ch717TxH	CH4H	DIO_8	N/C	Ch1_422R_L	N/C	CH4H	
A6L (140)	B6L (44)	C6L (157)	D6L (61)	13	Reserved	Ch717RxL	Reserved	DIO_9	GND	GND	GND	CH5L	
A6H (132)	B6H (36)	C6H (149)	D6H (53)	14	Reserved	Ch717RxH	Reserved	DGND_59	SHIELD	SHIELD	SHIELD	CH5H	
A7 (GND)	B7 (GND)	C7 (GND)	D7 (GND)	6	GND	GND	GND	GND	GND	GND	GND	GND	
SHIELD Pad	SHIELD Pad	SHIELD Pad	SHIELD Pad	1	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD	
				15	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	

Table 3-5 J1 and J2 Connector Pinouts for *M8K429RT5*, *M8K717*, *M8K825CAN*, *M8KDiscrete*, *M8KSerial* and *M8KMMSI* Modules

Table 3-6 lists the pinouts for the *M8K1553Px*, *M8K1760Px* and *M8K708* modules.

P1/P2 Mating Connector Through-hole Soldering Pad# and J1/J2 On-board Connector Pin# (in Parenthesis)				Twinax Adapter Cable Connector	9-Pin, D-Type, Male RT Lock Connector Pin# 1, 2, 3	Module Signal Names		
Modules 0 and 4	Modules 1 and 5	Modules 2 and 6	Modules 3 and 7			M8K1553Px/ M8K1760Px	M8K1553PxS/ M8K1760PxS	M8K708
A1L (100)	B1L (4)	C1L (102)	D1L (6)	Inner Sheath		BUS_AL	BUS_AL	CH0_L
A1H (108)	B1H (12)	C1H (110)	D1H (14)	Center Pin		BUS_AH	BUS_AH	CH0_H
A2L (98)	B2L (2)	C2L (117)	D2L (21)		8		RTA0	
A2H (106)	B2H (10)	C2H (125)	D2H (29)		7		RTA1	
A3L (115)	B3L (19)	C3L (119)	D3L (23)		6		RTA2	
A3H (123)	B3H (27)	C3H (127)	D3H (31)		5		RTA3	
A4L (138)	B4L (42)	C4L (142)	D4L (46)		4		RTA4	
A4H (130)	B4H (34)	C4H (134)	D4H (38)		3		RTAPRTY	
A5L (155)	B5L (59)	C5L (159)	D5L (63)	Inner Sheath		BUS_BL	BUS_BL	CH1_L
A5H (147)	B5H (51)	C5H (151)	D5H (55)	Center Pin		BUS_BH	BUS_BH	CH1_H
A6L (140)	B6L (44)	C6L (157)	D6L (61)		2		RTALOCK	
A6H (132)	B6H (36)	C6H (149)	D6H (53)		1		GND	
A7 (GND)	B7 (GND)	C7 (GND)	D7 (GND)					
SHIELD Pad	SHIELD Pad	SHIELD Pad	SHIELD Pad	Connector Body		SHIELD Pad	SHIELD Pad	SHIELD Pad

Table 3-6 J1 and J2 Connector Pinouts for *M8K1553Px*, *M8K1760Px* and *M8K708* Modules

1. For the *M8K1553PxS* and *M8K1760PxS* (single function module) only.
2. Pin 9 of the RT Lock Connector is not connected.
3. Not supplied with standard cable.

Table 3-7 lists the pinouts for the *M8KH009* and *M8K1553MCH* modules.

P1 Mating Connector Through-hole Soldering Pad# and J1 On-board Connector Pin# (in Parenthesis)				Twinax Adapter Cable Connector ¹	Module Signal Names	
Double-Sized Module in Module Positions 0 and 1		Double-Sized Module in Module Positions 2 and 3				
Module Position 0	Module Position 1	Module Position 2	Module Position 3		M8KH009	M8K1553MCH
	B1L (4)		D1L (6)	Inner Sheath	Data Bus A Low	Reserved
	B1H (12)		D1H (14)	Center Pin	Data Bus A High	Reserved
	B2L (2)		D2L (21)	Inner Sheath	Clock Bus A Low	Reserved
	B2H (10)		D2H (29)	Center Pin	Clock Bus A High	Reserved
	B3L (19)		D3L (23)		Shield	Reserved
	B3H (27)		D3H (31)		Ground	Reserved
A4L (138)		C4L (142)		Inner Sheath	Data Bus B Low	Bus B Low
A4H (130)		C4H (134)		Center Pin	Data Bus B High	Bus B High
A5L (155)		C5L (159)		Inner Sheath	Clock Bus B Low	Bus A Low
A5H (147)		C5H (151)		Center Pin	Clock Bus B High	Bus A High
A6L (140)		C6L (157)			Shield	Reserved
A6H (132)		C6H (149)			Reserved	Ground
A7 (Ground)	B7 (Ground)	C7 (Ground)	D7 (Ground)			
Shield Pad	Shield Pad	Shield Pad	Shield Pad	Connector Body	Shield Pad	Shield Pad

Table 3-7 J1 Connector Pinouts for Double-Sized *M8KH009* and *M8K1553MCH* Modules

- For more information on the adapter cable, see **3.4.2.2 Adapter Cable** on page 3-13.

Table 3-8 lists the pinouts for the *M8KADDA* module.

P1 Mating Connector Through-hole Soldering Pad# and J1 On-board Connector Pin# (in Parenthesis)					Module Signal Names					
Module 0	Module 1	Module 2	Module 3	HDB 15-pin Adapter Cable Connector Pin#	M8KADDA-P1 (DAC)		M8KADDA-P2 (ADC)		M8KADDA-P3 (DAC & ADC)	
					Single Ended	Differential	Single Ended	Differential	Single Ended	Differential
A1L(100)	B1L(4)	C1L(102)	D1L(6)	2	Channel 0 Output	Channel 0/1 Output High	Channel 0 Input	Channel 0/1 Input High	Channel 0 Output	Channel 0/1 Output High
A1H(108)	B1H(12)	C1H(110)	D1H(14)	3	Channel 1 Output	Channel 0/1 Output Low	Ground Reference Input	Channel 0/1 Input Low	Channel 1 Output	Channel 0/1 Output Low
A2L(98)	B2L(2)	C2L(117)	D2L(21)	4	Channel 2 Output	Channel 2/3 Output High	Channel 2 Input	Channel 2/3 Input High	Channel 2 Output	Channel 2/3 Output High
A2H(106)	B2H(10)	C2H(125)	D2H(29)	5	Channel 3 Output	Channel 2/3 Output Low	Ground Reference Input	Channel 2/3 Input Low	Channel 3 Output	Channel 2/3 Output Low
A3L(115)	B3L(19)	C3L(119)	D3L(23)	7	Channel 4 Output	Channel 4/5 Output High	Channel 4 Input	Channel 4/5 Input High	Channel 4 Input	Channel 4/5 Input High
A3H(123)	B3H(27)	C3H(127)	D3H(31)	8	Channel 5 Output	Channel 4/5 Output Low	Ground Reference Input	Channel 4/5 Input Low	Ground Reference Input	Channel 4/5 Input Low
A4L(138)	B4L(42)	C4L(142)	D4L(46)	9	Channel 6 Output	Channel 6/7 Output High	Channel 6 Input	Channel 6/7 Input High	Channel 6 Input	Channel 6/7 Input High
A4H(130)	B4H(34)	C4H(134)	D4H(38)	10	Channel 7 Output	Channel 6/7 Output Low	Ground Reference Input	Channel 6/7 Input Low	Ground Reference Input	Channel 6/7 Input Low
A5L(155)	B5L(59)	C5L(159)	D5L(63)	11	Channel 8 Output	Channel 8/9 Output High	Channel 8 Input	Channel 8/9 Input High	Channel 8 Input	Channel 8/9 Input High
A5H(147)	B5H(51)	C5H(151)	D5H(55)	12	Channel 9 Output	Channel 8/9 Output Low	Ground Reference Input	Channel 8/9 Input Low	Ground Reference Input	Channel 8/9 Input Low
A6L(140)	B6L(44)	C6L(157)	D6L(61)	13	Ground	Ground	Ground	Ground	Ground	Ground
A6H(132)	B6H(36)	C6H(149)	D6H(53)	14	Ground	Ground	Ground	Ground	Ground	Ground
A7 (Ground)	B7 (Ground)	C7 (Ground)	D7 (Ground)	6	Ground	Ground	Ground	Ground	Ground	Ground
Shield Pad	Shield Pad	Shield Pad	Shield Pad	1	Shield	Shield	Shield	Shield	Shield	Shield
				15	N/C	N/C	N/C	N/C	N/C	N/C

Table 3-8 J1 Connector Pinouts for the *M8KADDA* Module

3.4.2.1 External Signals

Table 3-9 lists the pinouts for the External Signals. Table 3-10 describes the External Signals.

An adapter cable with an External Signals Connector can be ordered from Excalibur. (It is not included with a standard adapter cable unless specifically ordered.) For more information on the adapter cable, see **3.4.2.2 Adapter Cable** on page 3-13.

External Signal Name	J1 Connector Pin# and Mating Connector Soldering Holes	9-Pin, D-Type, Male External Signals Connector Pin#
GND	A7, B7, C7, D7 (GND)	4, 7
SHIELD	SHIELD pad	9, Body
EXTTCLKO	A8 (83)	3
EXTTCLKI	A9 (84)	1
EXTTRSO _n	B8 (75)	8
EXTTRST _{In}	B9 (76)	2
N/C	C8 (86)	-
IRIGBIN	C9 (85)	6
N/C	D8 (78)	-
Reserved	D9 (77)	5

Table 3-9 J1 Connector Pinouts for External Signals

Signal	Description
GND	Provides ground reference for the digital signal connections.
SHIELD	Provided for a cables shield connection. This signal is connected to the case of the computer through the boards brackets or panel.
EXTTCLKO	Global Time Tag Clock TTL Output (1 MHz). This signal is the Global Clock that is supplied to all the modules for their Time Tags. Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules. ¹ The source of this clock is either the External Time Tag Clock EXTTCLKI ² or the Internal Time Tag Clock. See 2.5.7 Time Tag Clock Select Register on page 2-13 Time Tag Clock Select Register on page 2-13.
EXTTCLKI	External Time Tag Clock Input. This signal supplies an external global clock for the Time Tags of all the modules. Use this signal to synchronize the Time Tags that are implemented on the modules ¹ to other boards or systems. ² See 2.5.7 Time Tag Clock Select Register on page 2-13. This signal is a standard TTL input ($V_{ih_min} = 2.0V$) with a nominal 1 MHz clock of 50% duty cycle (+/-10%) in reference to the ground pin. Our internal Time Tag clock source has a 50 ppm stability.
EXTTRSON	Global Time Tag Reset TTL Output. This low active signal is activated by either the internal Global Time Tag signal (see 2.5.2 Software Reset Register on page 2-10) or from the External Time Tag signal (EXTTRSON). ² Use the signal to synchronize other boards or systems to the Time Tags that are implemented on the modules. ¹
EXTTRSTIn	External Time Tag Reset TTL Input. Use this low active pulsed signal (minimum 100 nsec.wide) to simultaneously reset the Time Tags of all the modules from an external source. Use the signal to synchronize these Time Tags to other boards or systems. ²
IRIGBIN	IRIG B120 Input. The signal should have the following specifications: B = 100 pulses per second (PPS), 10 msec count 1 = Sine wave carrier, amplitude modulated, with a 3:1 modulation ratio at 3Vpp typical amplitude 2 = 1 kHz carrier wave (1 msec resolution) 0 = Binary Coded Decimal (BCD) time-of-year code word Control Functions (CF) depending on the user application Straight Binary Second (SBS) of day (0 – 86400)

Table 3-10 External Signal Descriptions

1. See the manual for each module for a description of how the Time Tag clock is implemented, if used, for that module.
2. See **3.4.3.1 Synchronizing with an External Source** on page 3-16 and **3.4.3.2 Synchronizing Between Boards** on page 3-17.

3.4.2.2 Adapter Cable

An adapter cable can be ordered from Excalibur that terminates in separate connectors for each module installed on the board. Each connector carries the signals for one of the board's modules. The terminating connector for most modules is a standard 15-pin, high density, D-type, female connector. See Figure 3-7.

The *M8K1553Px*, *M8K1760Px* and *M8K708* modules terminate in two female twinax connectors (Trompeter CJ70 or equivalent) for Bus A and Bus B. See Figure 3-8. The cable is 0.5 meter in length. The twinax connector mates, for example, with a Trompeter PL75 male twinax connector. The mating connector is not supplied by Excalibur.

For boards with an *M8K1553PxS* module, an adapter cable can be ordered with an additional standard 9-pin, D-type, male connector for the RT Lock signals. See Figure 3-9. The RT Lock Connector does not come by default with the supplied cable.

The adapter cable can also be ordered with an External Signal Connector. The External Signal Connector is a standard 9-pin, D-type, male connector. See Figure 3-9.

Adapter cable pinouts are listed together with the J1 and J2 connector pinouts in **3.4.2 Communications I/O Connectors [J1 and J2]** on page 3-6.

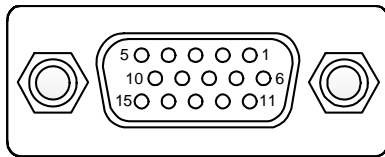


Figure 3-7 15-Pin Female I/O Connector – Front View

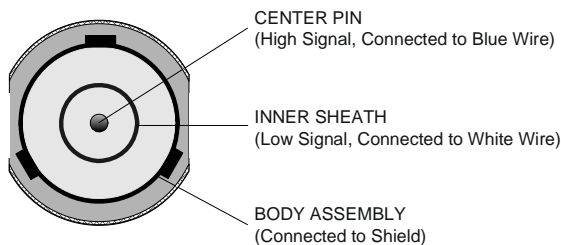


Figure 3-8 Twinax I/O Connector – Front View

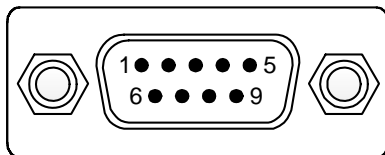


Figure 3-9 9-Pin Male Connector – Front View

3.4.2.3 Adapter Cable EXC-8000CON Assembly

The Adapter Cable has an EXC-8000CON assembly that mates with the J1/J2 connector. This describes how to assemble the connector containing the EXC-8000CON assembly. This is required if you want to build your own adapter cable.

To assemble the connector containing the EXC-8000CON assembly:

1. Figures 3-10 and 3-11 show both sides of the EXC-8000CON assembly. Figure 3-12 shows the rear side with the soldering hole numbers. Solder the adapter cable wires inside of the holes in Figure 3-12 according to the pinouts in Tables 3-5, 3-6 and 3-9.

Note: The soldering holes with circles around them are the **high** pins. For example, the soldering hole A3H (listed in Table 3-5) refers to the top-left soldering hole in section A. See Figure 3-12.

2. Fold the EXC-8000CON assembly and insert it into the connector hood. See figures 3-13 and 3-14. (These figure do not show the soldered wires.)
3. Close the connector hood and fasten the screws. See Figure 3-15.

Note: When connecting the adapter cable to the J1 or J2 connector, make sure to align the polarity mark on the EXC-8000CON connector with the polarity mark under the J1 or J2 connector. See Figures 3-2, 3-10 and 3-15.

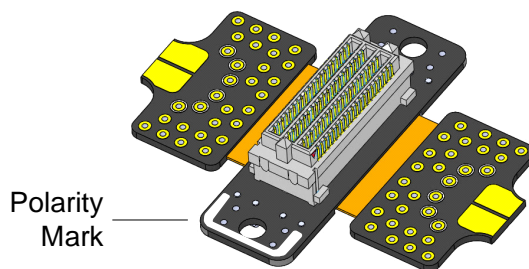


Figure 3-10 EXC-8000CON Assembly – Front View

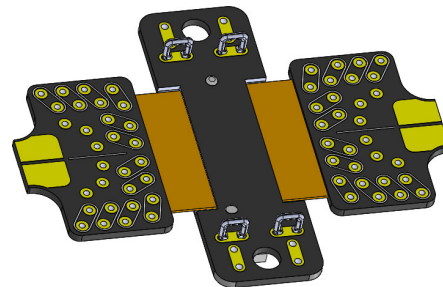


Figure 3-11 EXC-8000CON Assembly – Rear View

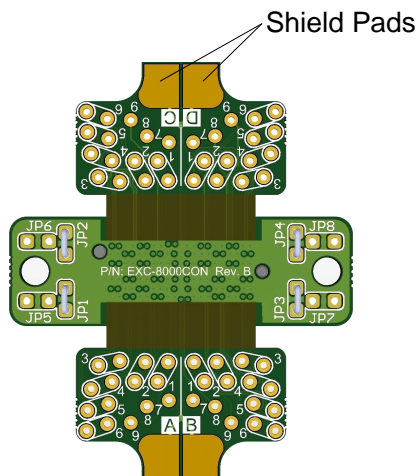


Figure 3-12 EXC-8000CON Assembly – Rear View with Soldering Holes

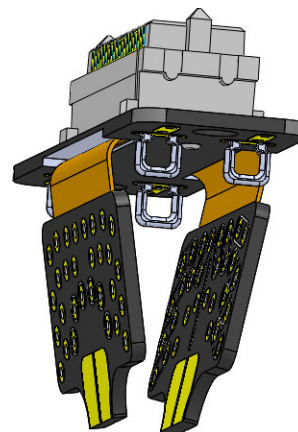


Figure 3-13 EXC-8000CON Assembly Folded

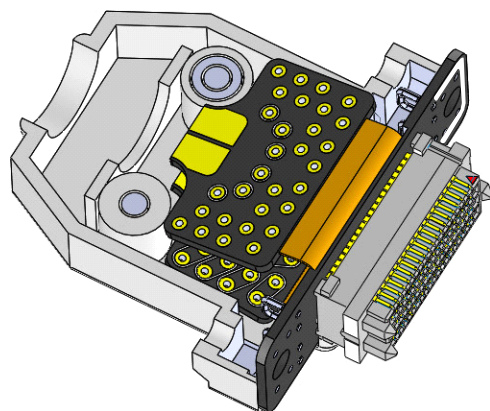


Figure 3-14 EXC-8000CON Assembly Inserted Into Hood

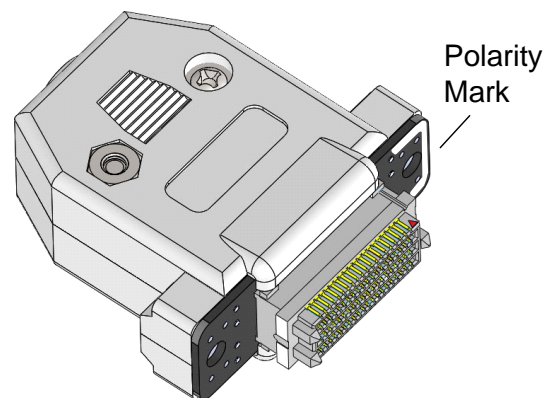


Figure 3-15 Connector Hood Closed

3.4.3 PCI Express Bus Edge Connector

Pin	Side B Connector		Side A Connector	
	Signal Name	Description	Signal Name	Description
1	(+12V)	N/C	PRSNT#1	Hot plug presence detect
2	(+12V)	N/C	(+12V)	N/C
3	RSVD	Reserved	(+12V)	N/C
4	GND	Ground	GND	N/C
5	(SMCLK)	N/C	(JTAG2)	N/C
6	(SMDAT)	N/C	(JTAG3)	N/C
7	GND	Ground	(JTAG4)	N/C
8	+3.3V	+3.3 volt power	(JTAG5)	N/C
9	(JTAG1)	N/C	+3.3V	+3.3 volt power
10	(3.3Vaux)	N/C	+3.3V	+3.3 volt power
11	(WAKE#)	N/C	PWRGD	Power good
CONNECTOR KEY				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock, differential pair
14	HSOp	Transmitter lane, differential pair	REFCLK-	
15	HSOn		GND	Ground
16	GND	Ground	HSIp	Receiver lane, differential pair
17	PRSNT#2	Hot plug detect	HSIn	
18	GND	Ground	GND	Ground

Table 3-11 PCI Express Bus Edge Connector Pinouts

N/C = Not connected on board

3.4.3.1 Synchronizing with an External Source

To synchronize a single board to an external system, the external clock source and the external reset must be connected to the EXTTCLKI and the EXTTRSTIn signals respectively.

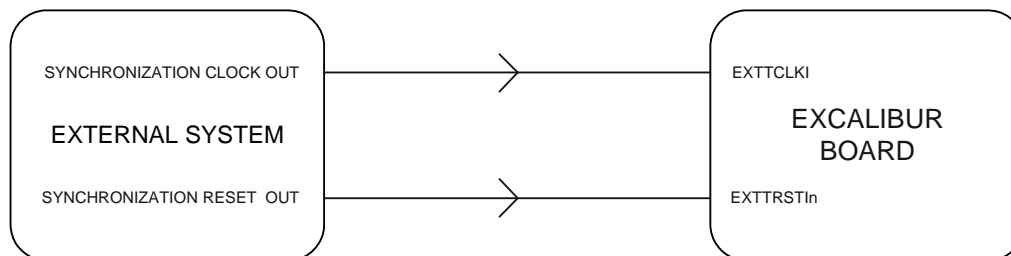


Figure 3-16 Synchronization of a Single Board to an External System

To synchronize an external system to a single *EXC-8000PCIe* board, the EXTTCLKO and the EXTTRSOIn signals need to be connected to the external clock source and the external reset respectively.

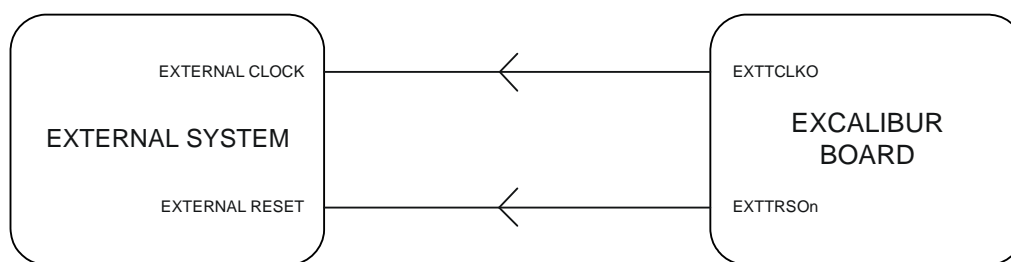


Figure 3-17 Synchronization of an External System to a Single Board

Warning: The synchronization clock and reset signals may be connected to multiple targets to achieve system wide synchronization.

3.4.3.2 Synchronizing Between Boards

To synchronize multiple boards the EXTTCLKO and the EXTTRSO_n signals of one board need to be connected to all the EXTTCLKI and the EXTTRSTIn signals respectively, of the remaining boards.

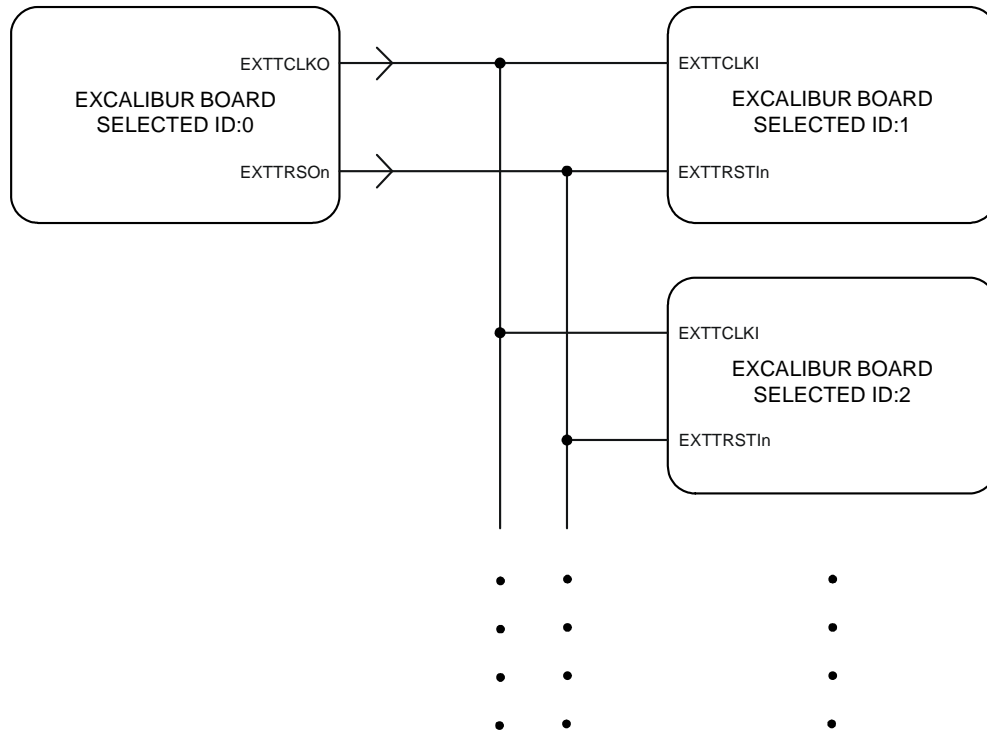


Figure 3-18 Synchronization Between Boards

3.5 Power Requirements

The standby power requirements, without any modules installed, are:

+3.3V @ 250mA

The power for the board is drawn from the PCI Express bus edge connector and the power for its modules is drawn from the power connector [J3]. See **3.4.1 SATA Connector [J3]** on page 3-5.

The final power requirements will depend on how many and which modules are installed. To calculate the exact board power requirements, see the specific module's user's manual.

4 Ordering Information

Chapter 4 explains which options to indicate when ordering.

Basic Part #	Option	Description
EXC-8000PCIe/xx		Multiprotocol carrier board for PCI Express (PCIe) compatible systems. Replace 'xx' with the module codes of the modules you want. See Table 4-2. For part number examples, see 4.1 Part Number Examples on page 4-3. When ordering the board without modules, leave the 'xx' in the part number. When ordering a module separate from a carrier board, use the module part # in Table 4-2. See the user's manual of the module for complete ordering information.
	-E	Extended temperature/ruggedized version. All the modules come with a ruggedized, extended temperature option (-40° to + 85°C).
	-001	With conformal coating
EXC-8000CON		J1/J2 mating connector assembly. Note: This is part of the adapter cable, but can also be ordered separately.

Table 4-1 Ordering Information

Note:

- For adapter cable part numbers, see **4.1 Adapter Cable Ordering Information** on page 4-4.
- External Loopback test connectors are available for most configurations. Contact Excalibur Sales for more information.

Table 4-2 lists the part numbers for the available modules.

Protocol Type	Module Part #	Module Code	Description
ARINC 429	M8K429RT5	A0	ARINC 429 module with 5 channels, software selectable as transmit or receive.
ARINC 708/453	M8K708	C0	ARINC 708/453 with 2 channels, software selectable as transmit or receive.
ARINC 717	M8K717-Nx	Nx	ARINC 717 module with 2 channels, one transmit and one receive. Replace 'Nx' with one of the following: N1 = HBP transmit channel N2 = BPRZ transmit channel
ARINC 825	M8K825CAN-S5	S5	ARINC 825 module with 5 channels.
MIL-STD-1553	M8K1553Px	F0	MIL-STD-1553 multi-function module. selectable as Transformer or Direct coupled via a DIP switch.
MIL-STD-1553 Monitor Only	M8K1553PxM	G0	MIL-STD-1553 multi-function module for monitoring only.

Table 4-2 Module Codes

Protocol Type	Module Part #	Module Code	Description
MIL-STD-1553 Single Function	M8K1553PxS	Tx	MIL-STD-1553 single function module. Replace 'Tx' with one of the following: T1 = PxS Transformer coupled mode T2 = PxS Direct coupled mode
MIL-STD-1553 Single Function Monitor Only	M8K1553PxSM	Vx	MIL-STD-1553 module for monitoring only. Replace 'Vx' with one of the following: V1 = PxS Transformer coupled mode V2 = PxS Direct coupled mode
MIL-STD-1553 MCH	M8K1553MCH	E0	MIL-STD-1553 MCH module. This is a double-sized module and occupies two modules locations. It can be installed in module locations 0–1, 2–3 or 4-5 (not 6–7).
MIL-STD-1760	M8K1760Px	L0	MIL-STD-1760 multi-function module, selectable as Transformer or Direct coupled via a DIP switch.
MIL-STD-1760 Monitor Only	M8K1760PxM	M0	MIL-STD-1760 multi-function module for monitoring only.
MIL-STD-1760 Single Function	M8K1760PxS	Hx	MIL-STD-1760 single function module. Replace 'Hx' with one of the following: H1 = PxS Transformer coupled mode H2 = PxS Direct coupled mode
MIL-STD-1760 Single Function Monitor Only	M8K1760PxSM	Kx	MIL-STD-1760 module for monitoring only. Replace 'Kx' with one of the following: K1 = PxS Transformer coupled mode K2 = PxS Direct coupled mode
MMSI	M8KMMSI-R5	R5	MMSI module with 5 EBR hub ports and 1 cBM port.
H009	M8KH009	D0	H009 interface module. This is a double-sized module and occupies two modules locations. It can be installed in module locations 0–1, 2–3 or 4-5 (not 6–7).
Discrete	M8KDiscrete	I0	Discrete module with 10 bi-directional Discretes with TTL (0 to 5 volts) or avionics (0 to 32 volts) voltage levels.
Serial	M8KSerial-Jx	Jx	Serial module with 2 channels, software selectable for RS-232 up to 3 Mbps and RS-422 and RS-485 up to 4 Mbps. Replace 'Jx' with one of the following: J1 = Channel 0 is RS-232; Channel 1 is RS-232 J2 = Channel 0 is RS-232; Channel 1 is RS-485 J3 = Channel 0 is RS-232; Channel 1 is RS-422 J4 = Channel 0 is RS-485; Channel 1 is RS-485 J5 = Channel 0 is RS-485; Channel 1 is RS-422 J6 = Channel 0 is RS-422; Channel 1 is RS-422
ADDA	M8KADDA	Px	A/D and D/A module. Replace 'Px' with one of the following: P1 = DAC outputs only, 10 single ended or 5 differential P2 = ADC inputs only, 5 single ended or 5 differential P3 = Combined DAC and ADC 4 single ended or 2 differential DAC outputs and 3 single ended or 3 differential ADC inputs

Table 4-2 Module Codes (Continued)

4.1 Part Number Examples

When ordering a board with a number of different protocol modules, the module codes must be in the following form:

EXC-8000PCIE/A0B1C0D0E0F0H0I0

The first module code (A0) in the part number is Module 0, the second (B1) is Module 1, and so on.

If one or more empty module locations are required in between other modules, insert an asterisk (*). Also, an asterisk (*) is required before the module code of a double-sized module for alignment purposes.

Example: EXC-8000PCIE/A0*F0

This is an *EXC-8000PCIE* board with:

An *M8K429RT5* module (A0) at module location 0

Module location 1 is empty (*)

An *M8K1553Px* module (F0) at module location 2

Module locations 3, 4, 5, 6 and 7 are empty

Example: EXC-8000PCIE/J2J3

This is an *EXC-8000PCIE* board with:

An *M8KSerial* module (J2) with channel 0 as RS-232 and channel 1 as RS-485 at module location 0

An *M8KSerial* module (J3) with channel 0 as RS-232 and channel 1 as RS-422 at module location 1

Module locations 2, 3, 4, 5, 6 and 7 are empty

Example: EXC-8000PCIE/J6T1*D0

This is a *EXC-8000PCIE* with:

An *M8KSerial* module (J6) with two RS-422 channel at module location 0.

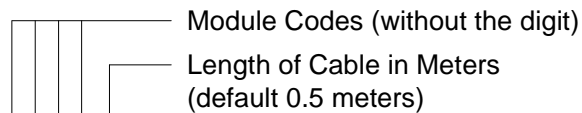
An *M8K1553PxS* single function Transformer coupled module (T1) at module location 1.

An *M8KH009* interface double-sized module (*D0) at module locations 2 and 3. An asterisk (*) is required before the module code of a double-sized module for alignment purposes.

Module locations 4, 5, 6 and 7 are empty

4.1 Adapter Cable Ordering Information

An adapter cable may be ordered using the **X8K-** prefix followed by the letter of each module code. Each adapter cable is for four modules, 0–3 or 4–7.



Adapter cable P/N: X8K-*MMMM*-*L*

Examples:

- X8K-AAFF-0.5** – Adapter cable for the EXC-8000PCIe/A0A0F0F0 board – 2 M8K429RT5 modules and 2 M8K1553Px modules – 0.5 meters in length.
- X8K-IRN(ES)-1** – Adapter cable for the EXC-8000PCIe/I0R5N1 board – 1 M8KDiscrete module, 1 M8KMMSI and 1 M8K717 module (HBP or BPRZ) – with an External Signals Connector, 1 meter in length.
- X8K-T(RT)CJ-0.3** – Adapter cable for the EXC-8000PCIe/T0C0J1 board – 1 M8K1553PxS module, 1 M8K708 and 1 M8KSerial module – with an RT Lock Connector for the M8K1553PxS module, 0.3 meters length.
- X8K-JT*D-0.5** Adapter cable for EXC-8000PCIe/J6T1*D0 board with 1 M8KSerial module, 1 M8K1553PxS single function module and 1 double-sized M8KH009 module, 50cm length.

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